

MOSTEK[®]

MD SERIES MICROCOMPUTER MODULES

Operations Manual

MDX-UMC
UNIVERSAL MEMORY
EXPANSION BOARD

Operation Manual

For

MDX-UMC

MK77759

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SECTION 1

GENERAL DESCRIPTION

1-1. INTRODUCTION

1-2. The MD series and the STD BUS were designed to satisfy the need for low cost OEM microcomputer modules. The STD BUS uses a motherboard interconnect system concept and is designed to handle any MD series card type in any slot. The modules for the STD BUS are compact 4.5 x 6.5 inches which provides for system partitioning by function (SRAM, EPROM, I/O). This smaller module size makes system packaging easier while increasing MOS-LSI densities provide high functionality per module.

1-3. The MD Series of OEM microcomputer boards and the STD BUS offer the most cost effective system configuration available to the OEM system designer.

1-4. GENERAL DESCRIPTION

1-5. The MDX-UMC is designed to be a universal memory expansion board for the MOSTEK MD SERIES of Z80 based microcomputers. It is designed to accept the following devices:

<u>EPROMS</u>	<u>SRAMS</u>	<u>ROMs</u>
2758 (1K x 8)	MK4118 (1K x 8)	MK34000 (2K x 8)
2716 (2K x 8)	MK4802 (2K x 8)	
2732 (4K x 8)		

The eight sockets on the MDX-UMC can be configured in pairs to accept any of the devices shown above to configure a SRAM board, EPROM board or a combination memory board made up of SRAMS and EPROM/ROMs.

The various population options are made possible by a jumper programmable memory decoder.

A jumper selectable wait state generator is provided for 4MHz operation. Wait states can be added on a socket for socket basis.

1-6. SPECIFICATIONS

1-7. ELECTRICAL SPECIFICATIONS

WORD SIZE

8 bits

MEMORY SIZE

<u>EPROM</u>	<u>RAM</u>	<u>ROM</u>
8K x 8 using 2758's	8K x 8 using MK4118's	16K x 8 using MK34000
16K x 8 using 2716's	16K x 8 using MK4802's	
32K x 8 using 2732's		

REQUIRED MEMORY DEVICE ACCESS TIME

CLOCK	MAXIMUM MEMORY DEVICE ACCESS TIME	
	NO WAIT STATES	ONE WAIT STATE
2.5MHz	530nS	930nS
4.0MHz	275nS	525nS

ADDRESS SELECTION

Selection of 4K, 8K, or 16K contiguous memory blocks to reside on any 4K boundary, i.e, 0000_H, 1000_H, 2000_H, 3000_H...etc.

PARALLEL BUS INTERFACE-STD BUS COMPATIBLE

Inputs one 74LS load max
 Bus Outputs I_{OH} = -15mA min. at 2.4 volts
 I_{OL} = 24mA min. at 0.5 volts

SYSTEM CLOCK

	<u>MIN</u>	<u>MAX</u>
MDX-UMC	250KHz	4MHz

POWER SUPPLY REQUIREMENTS

+5 volts ±5% at 0.450 A max. (Does not include memories)

OPERATING TEMPERATURE

0°C to 50°C

1-9. MECHANICAL SPECIFICATIONS

CARD DIMENSION

4.5 in. (11.43cm) high by 6.50 in. (16.51cm) long

0.48 in. (1.22cm) maximum profile thickness

0.062 in. (0.16cm) printed circuit board thickness

CONNECTORS

FUNCTION	CONFIGURATION	MATING CONNECTOR
STD BUS	56 pin dual read out 0.125 in. centers	Printed Circuit Viking 3VH28/1CE5 Wire wrap Viking 3VH28/1CND5 Solder Lug Viking 3VH28/1CN5

1-10. STD-Z80 BUS DESCRIPTION

BUS PIN	MNEMONIC	DESCRIPTION
1	+5V	+5Vdc system power
2	+5V	+5Vdc system power
3	GND	Ground-System signal ground and DC return
4	GND	Ground-System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	Data Bus (Tri-state, input/ output, active high). D0-D7 constitute an 8-bit bi-direc- tional data bus. The data bus is used for data exchange with memory and I/O devices.
8	D7	
9	D2	
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	Address Bus (Tri-state, output, active high). A0-A15 make up a 16 bit address bus. The address bus provides the address for memory (up to 65K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256
16	A15	
17	A6	
18	A14	
19	A5	
20	A13	
21	A4	
22	A12	
23	A3	
24	A11	

STD-Z80 BUS DESCRIPTION (contd)

BUS PIN	MNEMONIC	DESCRIPTION
25	A2	input or 256 output ports. A0
26	A10	is the least significant address
27	A1	bit. During refresh time, the lower
28	A9	7 bits contain a valid refresh
29	A0	address for dynamic memories.
30	A8	
31	/WR	Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Read (Tri-state, output, active low). RD indicates that the CPU wants to read data from memory or an I/O device. The address I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with /M1 signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-state output active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or memory write operation.

STD-Z80 BUS DESCRIPTION (contd)

BUS PIN	MNEMONIC	DESCRIPTION
35	/IOEXP	I/O Expansion, not used on MDX cards. (Normally strapped to ground on the MOSTEK motherboard).
36	/MEMEX	Memory Expansion, not used on Mostek MDX cards. (Normally strapped to ground on the MOSTEK motherboard)
37	/REFRESH	REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic 0 and the upper 8 bits of the address bus contains the I register.
38	/MCSYNC	Not generated on the MOSTEK MDX-CPU1. Can be generated by gating the following signals: /RD + /WR + /INTAK. By connecting a jumper on the MDX-CPU1, this line becomes /DEBUG (Input). /DEBUG is used in conjunction with the DDT-80 operating system on the MDX-DEBUG card, and the MDX-SST card for implementing a hardware single step function. When pulled low, the /DEBUG line will set an address modification latch which will force the upper three address lines A15, A14, and A13 to a logic 1. These address lines will remain at a logic 1 until reset by performing any I/O operation.
39	/STATUS1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the op code fetch cycle of an instruction. Note that during the ex-

STD-Z80 DESCRIPTION (contd)

BUS

PIN	MNEMONIC	DESCRIPTION
		ecution of two-byte opcodes /M1 will be generated as each op-code is fetched. These two-byte op-codes always begin with a CB _H , DD _H , ED _H , or FD _H . /M1 also occurs with IORQ to indicate an interrupt acknowledge cycle.
40	/STATUS 0	Not used on Mostek MDX cards.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.
42	/BUSRQ	Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the current CPU machine cycle is terminated and the /BUSAK signal is activated.
43	/INTAK	Interrupt acknowledge (Tri-state, output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus. The /INTAK signal is equivalent to an IORQ during an /M1.

STD-Z80 DESCRIPTION (contd)

BUS PIN	MNEMONIC	DESCRIPTION
44	/INTRQ	Interrupt Request (Input, active low). The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip flop (IFF) is enabled and if the BUSRQ signal is not active. When the CPU accepts the interrupt, an interrupt acknowledge signal /INTAK (IORQ during an M1) is sent out at the beginning of the next instruction.
45	/WAITRQ	Wait Request (Input, active low). Wait Request indicates to the CPU that the addressed memory or I/O device is not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU. Use of this signal postpones refresh as long as it held active.
46	/NMIRQ	Non-Maskable Interrupt Request (Input, negative edge triggered). The Non-Maskable Interrupt Request line has a higher priority than the /INTRQ line and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066 _H . The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending and that a /BUSRQ will override a /NMIRQ.

STD-Z80 DESCRIPTION (contd)

BUS PIN	MNEMONIC	DESCRIPTION
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated either from an external reset or the power on reset circuit. The system reset will occur only once per reset and will be approximately 2 microseconds in duration. A system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00 _H , set the R register to 00 _H , and set Interrupt Mode 0.
48	/PBRESET	Push Button Reset (Input, active low). The Push Button Reset will generate a debounced system reset.
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	/CNTRL	Not used on MOSTEK MDX cards.
*51	PCO	Priority Chain Output (Output, active high). The signal is used to form a priority-interrupt daisy chain when more than one interrupt-driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
*52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority-interrupt daisy chain when more than one interrupt-driven device is being used. A high level on this pin indicates that no other devices of higher priority are

STD-Z80 DESCRIPTION (contd)

BUS

PIN	MNEMONIC	DESCRIPTION
-----	----------	-------------

being serviced by a CPU interrupt service routine.

53	AUX GND	Auxiliary Ground (Bussed)
----	---------	---------------------------

54	AUX GND	Auxiliary Ground (Bussed)
----	---------	---------------------------

55	+12V	+12Vdc system power
----	------	---------------------

56	-12V	-12Vdc system power
----	------	---------------------

NOTES:

1. Input/Output references of each signal are made with respect to MDX-CPU1 module.
2. The following signals have pull-up resistors: /WR, /RD, /IORQ, /MEMRQ, /REFRESH, DEBUG, /M1, /BUSRQ, /INTAK, /INTRQ, /WAITRQ, /NMIRQ, /SYSRESET, /PBRESET, and /CLOCK. The value of the pull-up resistors are 1K except for /WAITRQ which is 500 ohms and /PBRESET which is 10K ohms. These resistors are located on the MDX-CPU1 module.

*The Mostek CCB, CC14 or CC28 Card cage is prioritized from left to right as viewed from the front with the component side of the boards to the left.

1-11. STD-Z80 ELECTRICAL BUS SPECIFICATION

BUS RECEIVERS

Logical Low: 0.8V maximum at -0.36mA

Logical High: 2.0V minimum at 20 microamperes

BUS DRIVERS

Logical Low: 0.5V maximum at 24mA

Logical High: 2.4V minimum at -15mA

Off State output Current (tri-state): ±100microamperes

RECOMMENDED BUS DRIVERS AND RECEIVERS

Bus Drivers: 74LS240, 74LS241, 74LS373, 74LS374, and 74LS244

Bus Receivers: 74LS240, 74LS241, and 74LS244

Bus Transceivers: 74LS245, 74LS242, and 74LS243

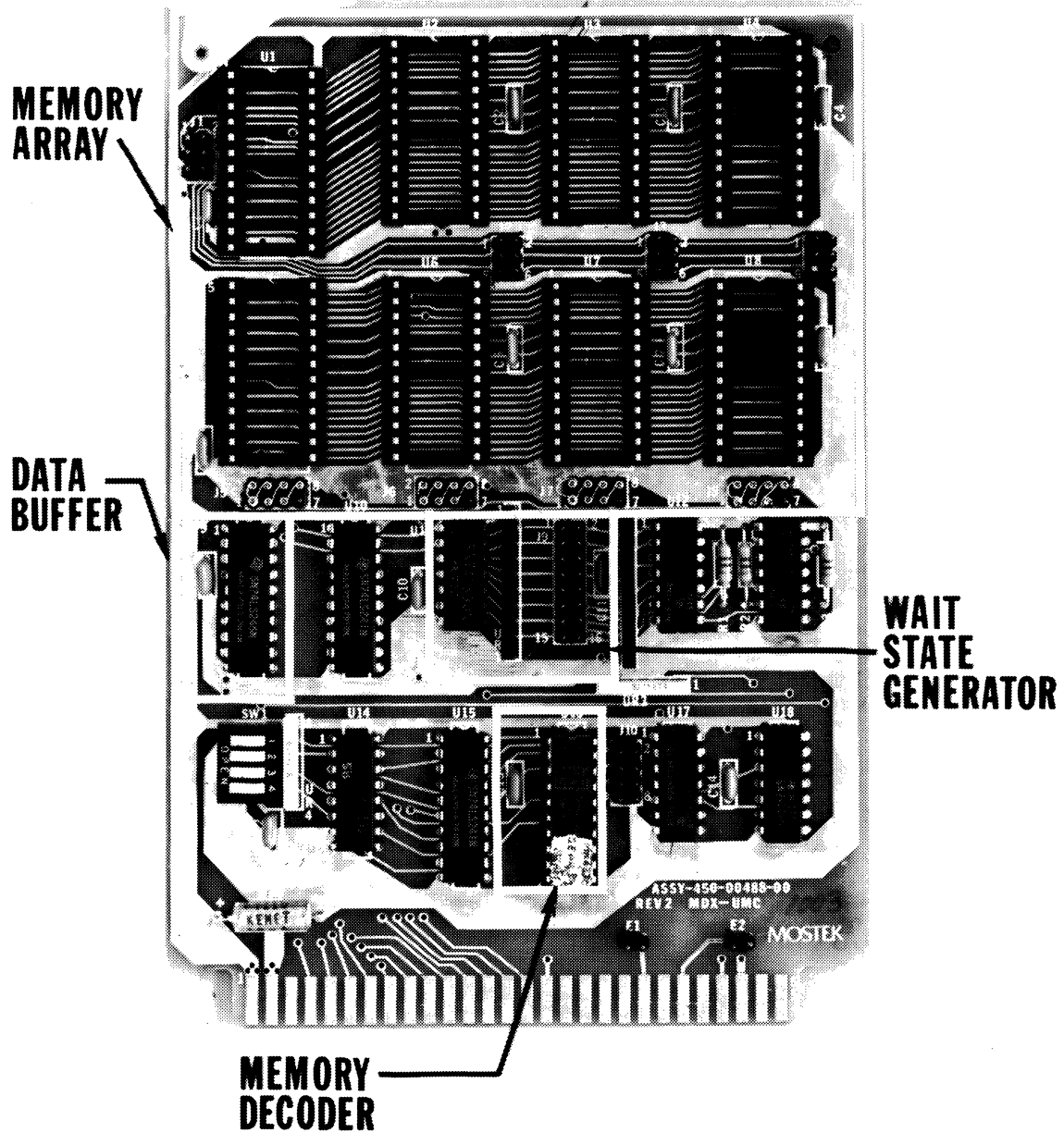
STD-Z80 BUS PIN-OUT

PIN	COMPONENT	PIN	CIRCUIT
	SIDE MNEMONIC		SIDE MNEMONIC
1	+5V	2	+5V
3	GND	4	GND
5	-5V	6	-5V
7	D3	8	D7
9	D2	10	D6
11	D1	12	D5
13	D0	14	D4
15	A7	16	A15
17	A6	18	A14
19	A5	20	A13
21	A4	22	A12
23	A3	24	A11

STD-Z80 BUS PIN-OUT

COMPONENT		CIRCUIT	
PIN	SIDE MNEMONIC	PIN	SIDE MNEMONIC
25	A2	26	A10
27	A1	28	A9
29	A0	30	A8
31	/WR	32	/RD
33	/IORQ	34	/MEMRQ
35	/IOEXP	36	/MEMEX
37	/REFRESH	38	/MCSYNC
39	/STATUS 1	40	/STATUS 0
41	/BUSAK	42	/BUSRQ
43	/INTAK	44	/INTRQ
45	/WAITRQ	46	/NMIRQ
47	/SYSRESET	48	/PBRESET
49	/CLOCK	50	/CNTRL
51	PC0	52	PCI
53	AUX GND	54	AUX GND
55	+12V	56	-12V

FIGURE 1-1. BOARD PHOTO WITH OVERLAY



SECTION 2

FUNCTIONAL DESCRIPTION

2-1. INTRODUCTION

2-2. The MDX-UMC block diagram shown in Figure 2-1 provides a low cost way to expand memory for the MDX system. The major functions of the MDX-UMC are shown in Figure 2-1 and will be explained below.

2-3. **MEMORY ARRAY.** The memory array consists of up to 8 RAMs, EPROMs or ROM Memories. The Memories are organized into an array of eight devices with each device contributing one byte to an addressable location.

2-4. **MEMORY DECODE AND CONTROL.** The memory decode and control section is responsible for generating the necessary chip select and output enable signals for the memory array's. Timing within the memory decode and control section is derived from the STD-Z80 BUS control signals, /MEMRQ, /RD, and /CLOCK.

2-5. **ADDRESS BUFFER.** The address buffer is responsible for isolating the STD-Z80 address bus from the memory array.

2-6. **DATA BUFFER.** The data buffer isolates the memory array from the data bus and is controlled by the memory decode and control section.

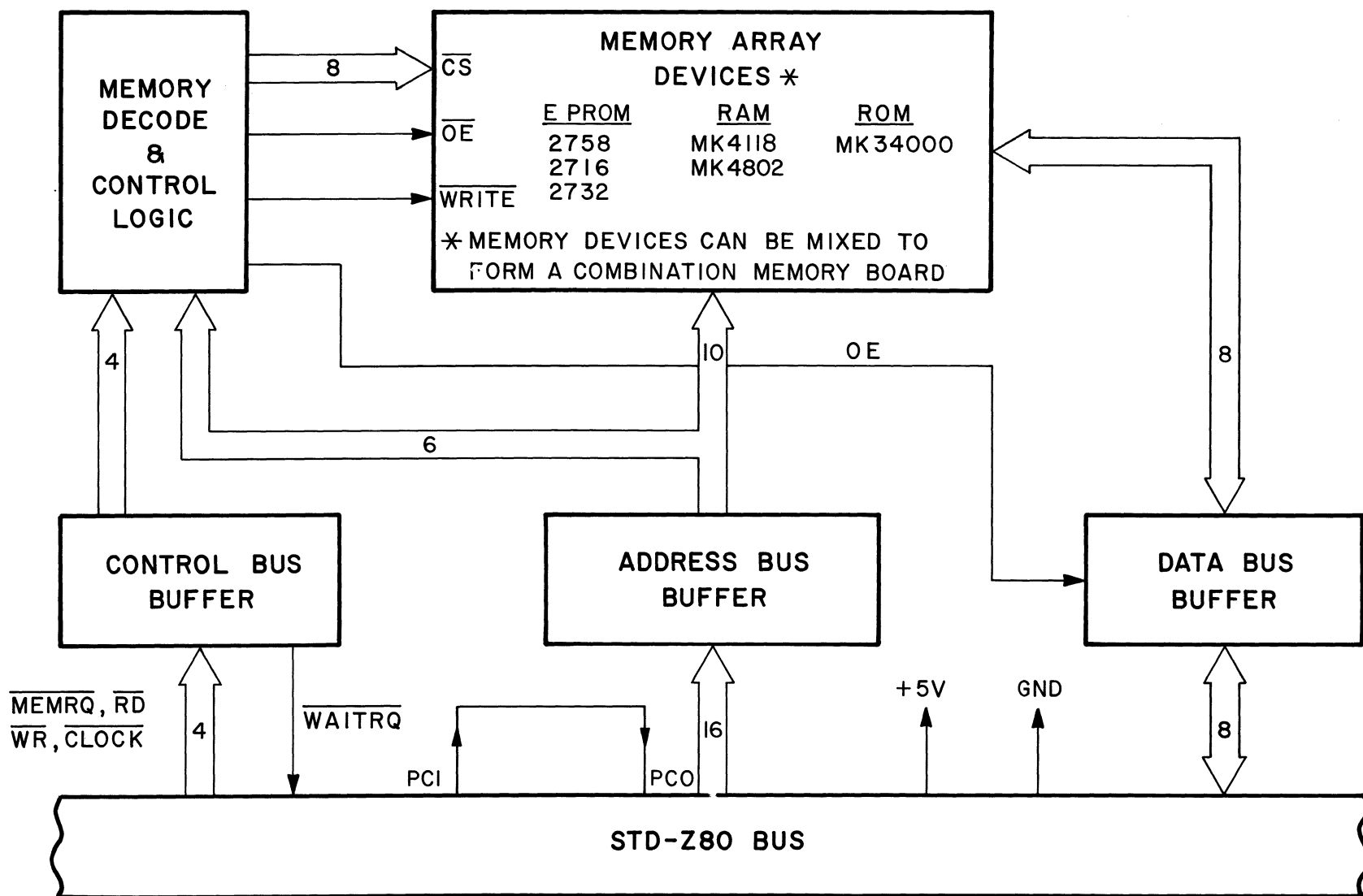


FIGURE 2-1. MDX-UMC BLOCK DIAGRAM

SECTION 3

UTILIZATION

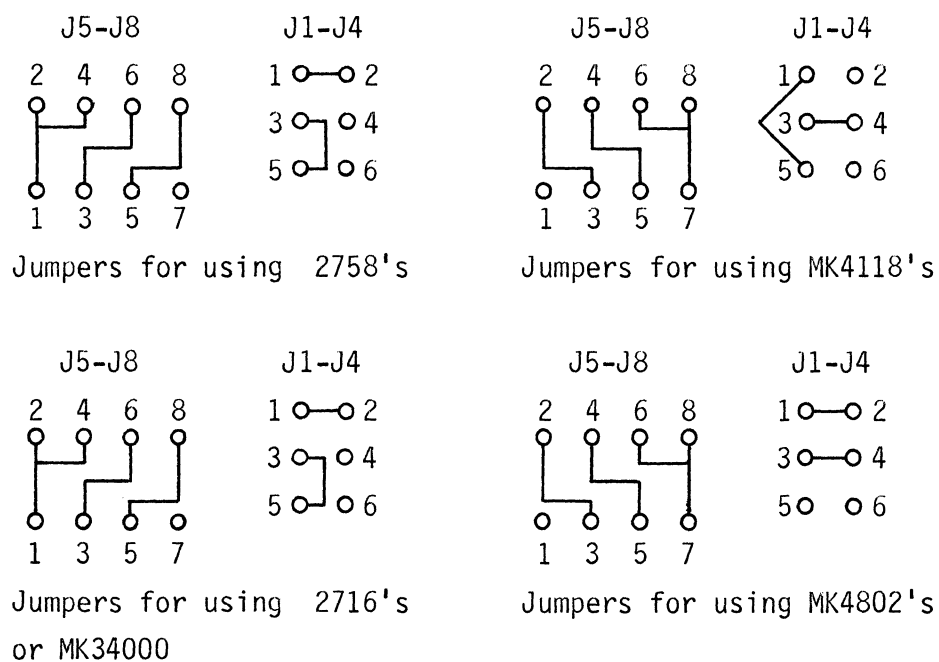
3-1. INTRODUCTION

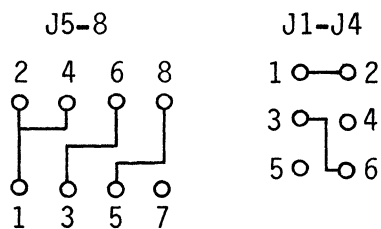
3-2. This section will describe the various jumper options and switch settings for the MDX-UMC.

3-3. MEMORY DEVICE SELECTION JUMPERS

3-4. Figure 3-1 shows how J1-J8 are configured to accomodate the various RAMs, EPROMs, and ROM's.

FIGURE 3-1. JUMPER CONFIGURATIONS





Jumpers for using 2732's

3-5. Table 3-1 shows how the jumpers J1-J8 are related to memory sockets. It is important to note that the memory sockets are configured in pairs for a particular memory device!

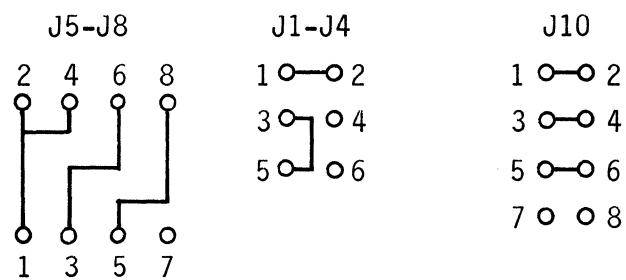
TABLE 3-1
MEMORY DEVICE JUMPERS

MEMORY SOCKETS	CONTROLLING JUMPERS
U4, U8	J4, J8
U3, U7	J3, J7
U2, U6	J2, J6
U1, U5	J1, J5

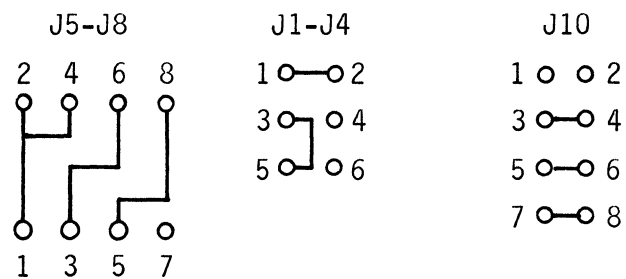
3-6. MEMORY SIZE SELECTION JUMPERS

3-7. The size of the MDX-UMC memory can be adjusted by the use of J10. Before configuring the J10 jumpers, be sure that the memory device jumpers are in place as described in 3-3. Figure 3-2 shows the possible combinations of J10 versus memory size.

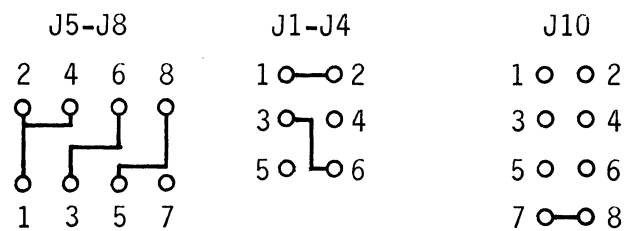
FIGURE 3-3. MEMORY DEVICE AND SIZE JUMPER EXAMPLES



8K x 8 EPROM MEMORY USING 2758's

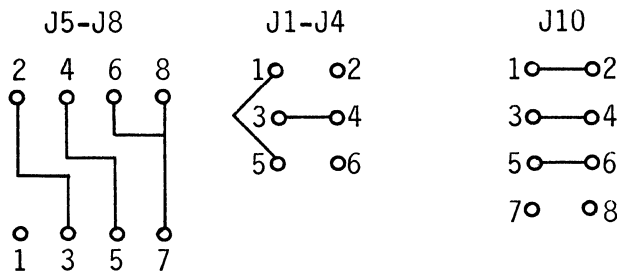


16K x 8 EPROM MEMORY USING 2716's or MK34000's

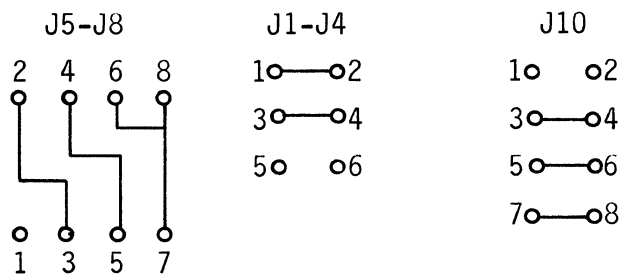


32K x 8 EPROM MEMORY USING 2732's

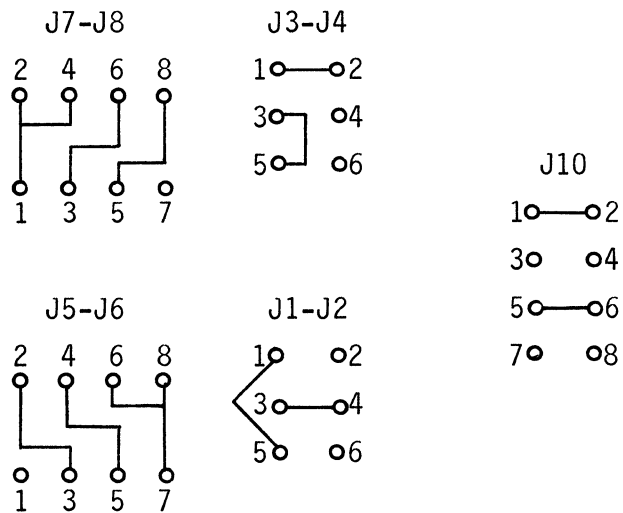
FIGURE 3-3. (contd)



8K x 8 SRAM USING MK4118's



16K x 8 SRAM USING MK4802's



COMBINATION 8K x 8 EPROM AND 4K x 8 SRAM (See Figure 3-2 for MEMORY ALLOCATION)

3-8. MEMORY DECODING

3-9. Memory decoding for the MDX-UMC is on 4K boundaries i.e. 0000_H, 1000_H, 2000_H etc. The starting address for the MDX-UMC is selected by a four position jumper block, J11. Table 3-1 shows the jumper setting for J11 versus starting address.

TABLE 3-2
MEMORY DECODING

STARTING ADDRESS	J11 JUMPER POSITION
	1 2 3 4
	MSB - 0 0 0 0 - LSB
0 0 0 0	1 1 1 1
1 0 0 0	1 1 1 0
2 0 0 0	1 1 0 1
3 0 0 0	1 1 0 0
4 0 0 0	1 0 1 1
5 0 0 0	1 0 1 0
6 0 0 0	1 0 0 1
7 0 0 0	1 0 0 0
8 0 0 0	0 1 1 1
9 0 0 0	0 1 1 0
A 0 0 0	0 1 0 1
B 0 0 0	0 1 0 0
C 0 0 0	0 0 1 1
D 0 0 0	0 0 1 0
E 0 0 0	0 0 0 1
F 0 0 0	
0 = JUMPERED	1 = OPEN

3-10. WAIT STATE GENERATOR

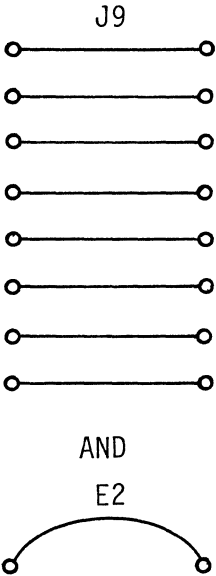
3-11. Since most MOS EPROM's cannot meet the required 275ns access to allow the MDX-UMC to work at 4MHz, a one wait state generator has been provided. Figure 3-4 shows how to enable the wait state generator, for each memory socket.

FIGURE 3-4. ENABLING THE WAIT STATE GENERATOR

ADD ONE WAIT STATE FOR MEMORY IN SOCKET	CONNECT JUMPER BETWEEN
U4	J9 15 to 16
U8	J9 13 to 14
U3	J9 11 to 12
U7	J9 9 to 10
U2	J9 7 to 8
U6	J9 5 to 6
U1	J9 3 to 4
U5	J9 1 to 2

3-11. An example of how to enable the wait states for every memory socket is shown in figure 3-5.

FIGURE 3-5. EXAMPLE FOR ENABLING ONE WAIT STATE FOR EACH MEMORY SOCKET



APPENDIX A

FACTORY REPAIR

LIMITED WARRANTY

APPENDIX A

FACTORY REPAIR SERVICE

In the event that difficulty is encountered with this unit, it may be returned directly to MOSTEK for repair. This service will be provided free of charge if the unit is returned within 90 days of purchase. However, units which have been modified or abused in any way either will not be accepted for service or will be repaired at the owner's expense.

When returning the circuit board, place it inside the conductive plastic bag in which it was delivered in order to protect the MOS device from electrostatic discharge during shipment. ENCLOSE a letter containing the following information with the returned circuit board.

Name, address, and phone number of purchaser

Date and place of purchase

Brief description of the difficulty

Mail a copy of this letter SEPARATELY to:

MOSTEK Corporation

Microcomputer Service Manager

1215 West Crosby Road

Carrollton, Texas 75006

Securely package and mail the circuit board, prepaid and insured to:

MOSTEK Corporation

Microcomputer Service Department

1215 West Crosby Road

Carrollton, Texas 75006

LIMITED WARRANTY

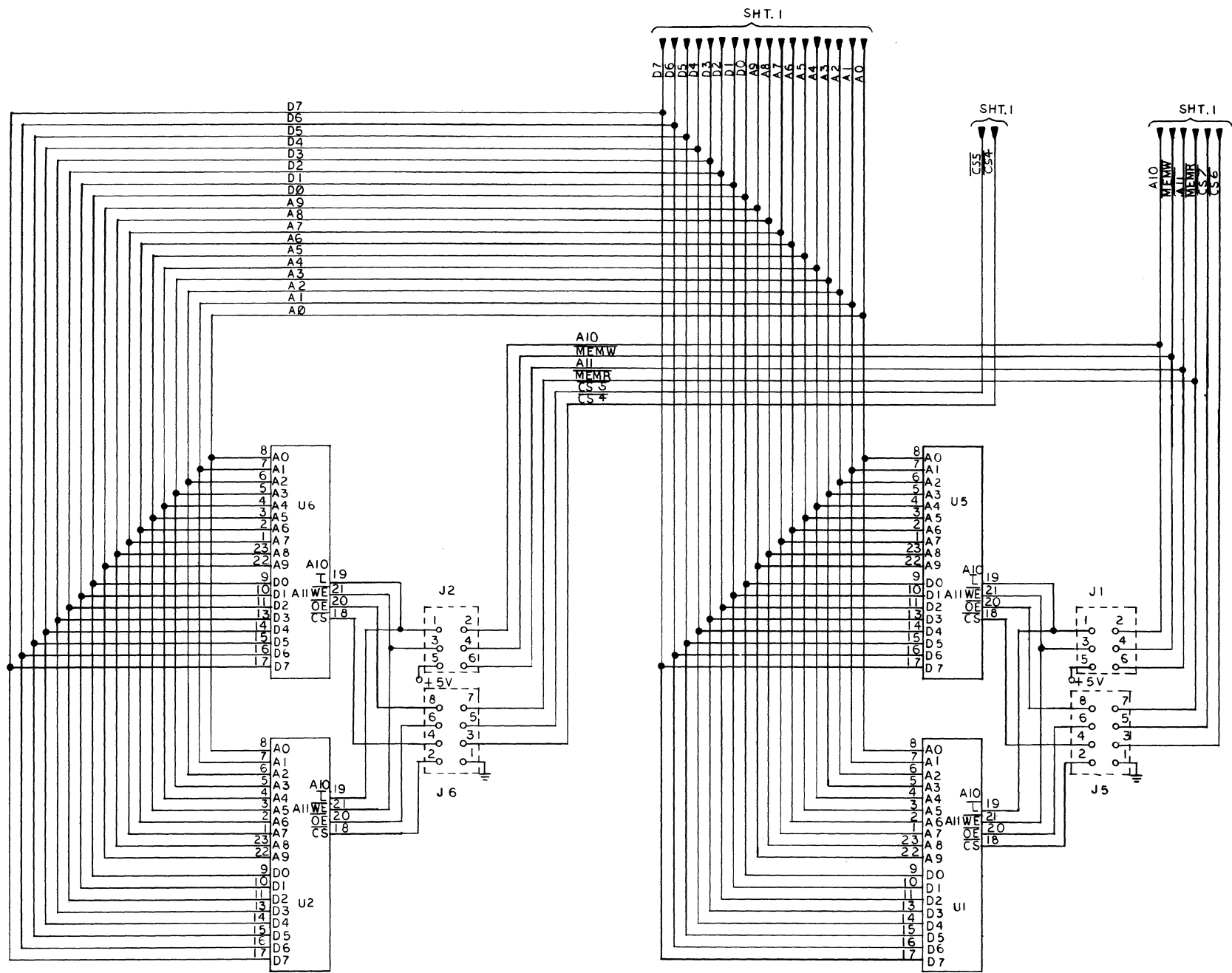
MOSTEK warrants this product against defective materials and workmanship for a period of 90 days.

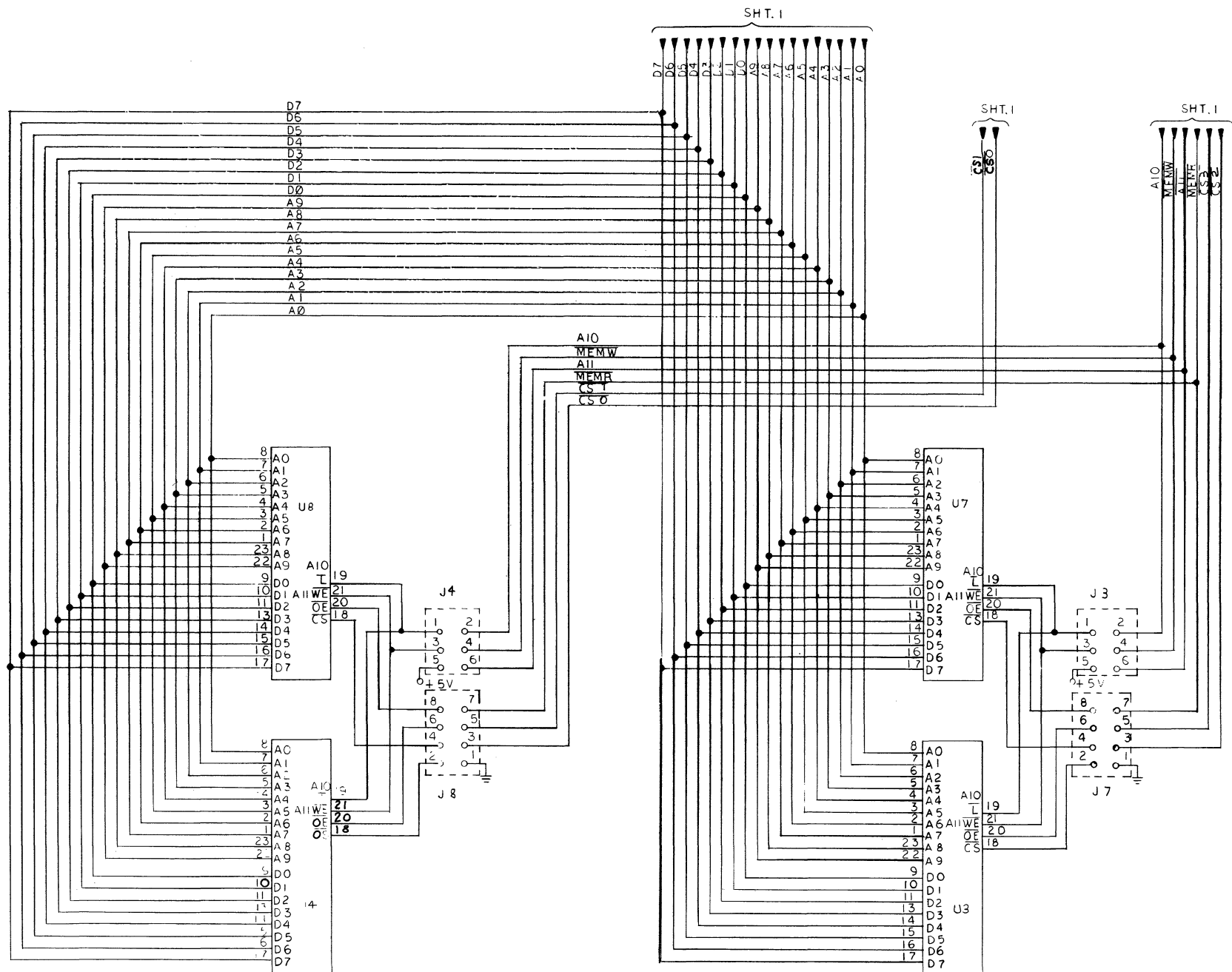
This warranty does not apply to any product that has been subjected to misuse, accident, improper installation, improper application, or improper operation, nor does it apply to any product that has been repaired or altered by other than MOSTEK personnel.

There are no warranties which extend beyond those herein specifically given.

APPENDIX B

SCHEMATIC DIAGRAMS



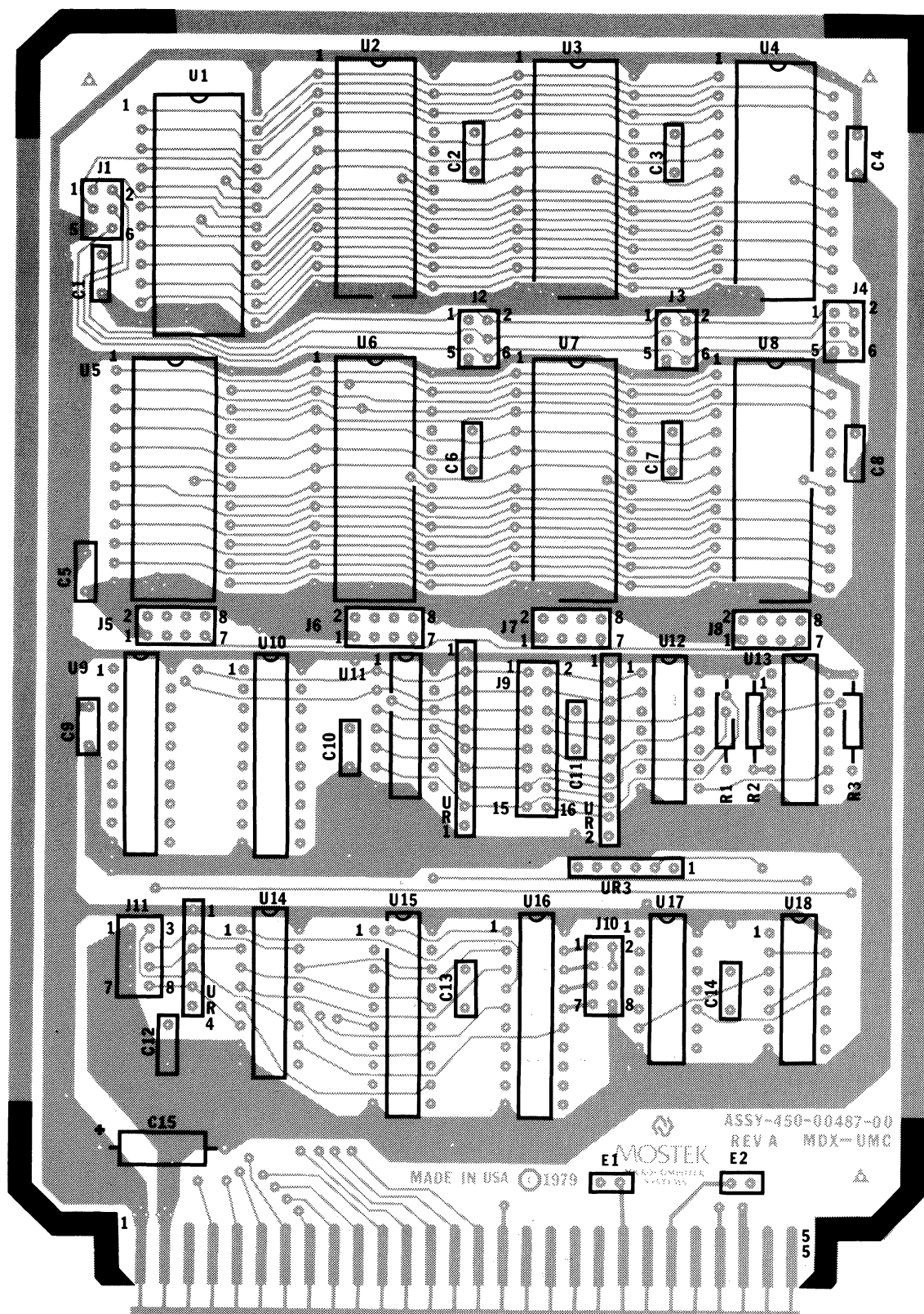


APPENDIX C

ASSEMBLY DRAWING

PARTS LIST

ASSEMBLY DRAWING



PARTS LIST

MDX-UMC

MK 77759

PART NO	QTY.	DESCRIPTION	REFERENCE DESTNATOR	USED ON
0C00001		ASSY 450-C0487-A05 REV A	AZ:MDX-UMC	77759
0C00002		SCH 450-C0488-00 REV A	AZ:MDX-UMC	77759
4610193	1	FAB 450-C0486-00 REV A	AZ:PC BOARD MDX-UMC	77759
4280155	1	EJECTOR CARD EDGE	B	77759
4150111	14	.1MF CAP	C1-C14	77759
4150140	1	15MF TANT ELECTRO. CAP	C15	77759
4210159	4	6 PIN HEADER	J1-J4	77759
4210239	6	8 PIN HEADER	J5-J8,J10,J11	77759
4210143	1	16 PIN HEADER	J9	77759
4470065	3	470 OHM 5% 1/4W RES	R1,R2,R3	77759
4313508	1	IC TTL 74LS245	U 9	77759
4313409	2	IC TTL 74LS241	U10,U15	77759
4313410	1	IC TTL 74LS30	U11	77759
4313315	1	IC TTL 74S30	U12	77759
4313317	1	IC TTL 74S38	U13	77759
4314334	1	IC TTL 74LS283	U14	77759
4313768	1	IC TTL MK6271	U16	77759
4313291	1	IC TTL 74LS14	U17	77759
4313266	1	IC TTL 74S74	U18	77759
4470174	1	1C PIN SIP 1KOHM	UR1	77759
4470175	1	1C PIN SIP 4.7KOHM	UR2	77759
4470202	2	6 PIN SIP 4.7KOHM	UR3,UR4	77759
4620018	8	24 PIN DIP SOCKET	X1-X8	77759
4620070	1	20 PIN DIP SOCKET	X16	77759
5025266	1	TRAVELER WIP	Z: NOTE IN HOUSE USE ONLY	77759
5013004	2	BAG ANTISTATIC	Z: SHIPPED NOT ASSEMBLED	77759
5013204	1	BOX SHIPPING	Z: SHIPPED NOT ASSEMBLED	77759
::::::::::		SHIPPING LIST MDX-UMC	////////////////////////////////////	77759
MK77759	1	MDX-UMC BOARD	////////////////////////////////////	77759
MK78409	1	FACTORY REPAIR SHEET	////////////////////////////////////	77759
MK78410	1	LIMITED WARREANTY SHEET	////////////////////////////////////	77759
MK78425	1	ANTISTATIC NOTICE	////////////////////////////////////	77759
MK79667	1	MDX-UMC OPS MANUAL	////////////////////////////////////	77759
MK79763	1	MD SERIES BROCHURE	////////////////////////////////////	77759

FOR JUMPER OPTIONS SEE MDX-UMC
OPS MANUAL MK 79667

APPENDIX D

PROM DECODER LISTING

UMC PROM DECODER LISTING
(512 x 8 PROM)

000	FE	020	FE	040	FE	060	FE	080	FE	0A0	FE	0C0	FE	0E0	FF
001	FD	021	FD	041	FE	061	FE	081	FE	0A1	FE	0C1	FE	0E1	FF
002	FB	022	FB	042	FD	062	FD	082	FD	0A2	FD	0C2	FD	0E2	FF
003	F7	023	F7	043	FD	063	FD	083	FD	0A3	FD	0C3	FD	0E3	FF
004	FF	024	EF	044	FB	064	FB	084	FB	0A4	FB	0C4	FB	0E4	FF
005	FF	025	DF	045	FB	065	FB	085	FB	0A5	FB	0C5	FB	0E5	FF
006	FF	026	BF	046	F7	066	F7	086	F7	0A6	F7	0C6	F7	0E6	FF
007	FF	027	7F	047	F7	067	EF	087	EF	0A7	F7	0C7	F7	0E7	FF
008	FF	028	FF	048	FF	068	DF	088	FF	0A8	E7	0C8	EF	0E8	FF
009	FF	029	FF	049	FF	069	FF	089	FF	0A9	D7	0C9	EF	0E9	FF
00A	FF	02A	FF	04A	FF	06A	FF	08A	FF	0AA	BF	0CA	DF	0EA	FF
00B	FF	02B	FF	04B	FF	06B	FF	08B	FF	0AB	7F	0CB	BF	0EB	FF
00C	FF	02C	FF	04C	FF	06C	FF	08C	FF	0AC	FF	0CC	FF	0EC	FF
00D	FF	02D	FF	04D	FF	06D	FF	08D	FF	0AD	FF	0CD	FF	0ED	FF
00E	FF	02E	FF	04E	FF	06E	FF	08E	FF	0AE	FF	0CE	FF	0EE	FF
00F	FF	02F	FF	04F	FF	06F	FF	08F	FF	0AF	FF	0CF	FF	0EF	FF
010	FF	030	FF	050	FF	070	FF	090	FF	0B0	FF	0D0	FF	0F0	FF
011	FF	031	FF	051	FF	071	FF	091	FF	0B1	FF	0D1	FF	0F1	FF
012	FF	032	FF	052	FF	077	FF	092	FF	0B2	FF	0D2	FF	0F2	FF
013	FF	033	FF	053	FF	073	FF	093	FF	0B3	FF	0D3	FF	0F3	FF
014	FF	034	FF	054	FF	074	FF	094	FF	0B4	FF	0D4	FF	0F4	FF
015	FF	035	FF	055	FF	075	FF	095	FF	0B5	FF	0D5	FF	0F5	FF
016	FF	036	FF	056	FF	076	FF	096	FF	0B6	FF	0D6	FF	0F6	FF
017	FF	037	FF	057	FF	077	FF	097	FF	0B7	FF	0D7	FF	0F7	FF
018	FF	038	FF	058	FF	078	FF	098	FF	0B8	FF	0D8	FF	0F8	FF
019	FF	039	FF	059	FF	079	FF	099	FF	0B9	FF	0D9	FF	0F9	FF
01A	FF	03A	FF	05A	FF	07A	FF	09A	FF	0BA	FF	0DA	FF	0FA	FF
01B	FF	03B	FF	05B	FF	07B	FF	09B	FF	0BC	FF	0DB	FF	0FB	FF
01C	FF	03C	FF	05C	FF	07C	FF	09C	FF	0BC	FF	0DC	FF	0FC	FF
01D	FF	03D	FF	05D	FF	07D	FF	09D	FF	0BD	FF	0DD	FF	0FD	FF
01E	FF	03E	FF	05E	FF	07E	FF	09E	FF	0BE	FF	0DE	FF	0FE	FF
01F	FF	03F	FF	05F	FF	07F	FF	09F	FF	0BF	FF	0DF	FF	0FF	FF

UMC PROM DECODER USING (contd)
(512 x 8 PROM)

100	FE	120	FE	140	FE	160	FE	180	FE	1A0	FE	1C0	FE	1E0	FF
101	FE	121	FE	141	FE	161	FE	181	FE	1A1	FE	1C1	FE	1E1	FF
102	FD	122	FE	142	FE	162	FE	182	FE	1A2	FE	1C2	FE	1E2	FF
103	FD	123	FE	143	FE	163	FE	183	FE	1A3	FE	1C3	FE	1E3	FF
104	FB	124	FD	144	FD	164	FD	184	FD	1A4	FD	1C4	FD	1E4	FF
105	FB	125	FB	145	FD	165	FD	185	FD	1A5	FD	1C5	FD	1E5	FF
106	F7	126	F7	146	FD	166	FD	186	FD	1A6	FD	1C6	FD	1E6	FF
107	F7	127	EF	147	FD	167	FD	187	FD	1A7	FD	1C7	FD	1E7	FF
108	EF	128	FF	148	FB	168	FB	188	FB	1A8	FB	1C8	FB	1E8	FF
109	EF	129	FF	149	F7	169	FB	189	FB	1A9	FB	1C9	FB	1E9	FF
10A	DF	12A	FF	14A	EF	16A	FB	18A	F7	1AA	FB	1CA	FB	1EA	FF
10B	DF	12B	FF	14B	DF	16B	FB	18B	F7	1AB	FB	1CB	FB	1EB	FF
10C	BF	12C	FF	14C	FF	16C	F7	18C	EF	1AC	F7	1CC	F7	1EC	FF
10D	BF	12D	FF	14D	FF	16D	EF	18D	EF	1AD	F7	1CD	F7	1ED	FF
10E	7F	12E	FF	14E	FF	16E	DF	18E	DF	1AE	EF	1CE	F7	1EE	FF
10F	7F	12F	FF	14F	FF	16F	BF	18F	DF	1AF	EF	1CF	F7	1EF	FF
110	FF	130	FF	150	FF	170	FF	190	BF	1B0	DF	1D0	EF	1F0	FF
111	FF	131	FF	151	FF	171	FF	191	BF	1B1	DF	1D1	EF	1F1	FF
112	FF	132	FF	152	FF	172	FF	192	7F	1B2	BF	1D2	EF	1F2	FF
113	FF	133	FF	153	FF	173	FF	193	7F	1B3	BF	1D3	EF	1F3	FF
114	FF	134	FF	154	FF	174	FF	194	FF	1B4	FF	1D4	DF	1F4	FF
115	FF	135	FF	155	FF	175	FF	195	FF	1B5	FF	1D5	DF	1F5	FF
116	FF	136	FF	156	FF	176	FF	196	FF	1B6	FF	1D6	DF	1F6	FF
117	FF	137	FF	157	FF	177	FF	197	FF	1B7	FF	1D7	DF	1F7	FF
118	FF	138	FF	158	FF	178	FF	198	FF	1B8	FF	1D8	BF	1F8	FF
119	FF	139	FF	159	FF	179	FF	199	FF	1B9	FF	1D9	BF	1F9	FF
11A	FF	13A	FF	15A	FF	17A	FF	19A	FF	1BA	FF	1DA	BF	1FA	FF
11B	FF	13B	FF	15B	FF	17B	FF	19B	FF	1BB	FF	1DB	BF	1FB	FF
11C	FF	13C	FF	15C	FF	17C	FF	19C	FF	1BC	FF	1DC	7F	1FC	FF
11D	FF	13D	FF	15D	FF	17D	FF	19D	FF	1BD	FF	1DD	7F	1FD	FF
11E	FF	13E	FF	15E	FF	17E	FF	19E	FF	1BE	FF	1DE	7F	1FE	FF
11F	FF	13F	FF	15F	FF	17F	FF	19F	FF	1BF	FF	1DF	7F	1FF	FF

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